1. A semiconductor device comprising:

a. a semiconductor substrate;

b. at least one first doped region in said semiconductor substrate forming at least one source;

c. at least one second doped region in said semiconductor substrate forming at least one drain;

d. a first connectivity layer having at least one first runner and at least one second runner, wherein said at least one first runner is operatively connected to said at least one first doped region and said at least one second runner is operatively connected to said at least one second doped region;

e. a second connectively layer operatively connected to said first connectively layer and having at least one third runner and at least one fourth runner, wherein said at least one third runner is operatively connected to said at least one first runner and said at least one fourth runner is operatively connected to said at least one second runner;

f. a third connectively layer having at least one first pad operatively connected to said at least one third runner and at least one second pad operatively connected to said at least one fourth runner.

2. A semiconductor device of claim 1 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

3. A semiconductor device of claim 2 wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

4. A semiconductor device of claim 2 wherein said at least one first pad is interleaved with said at least one second pad.

5. A semiconductor device of claim 1 wherein said at least one first doped region is a source for a transistor and said at least one second doped region is a drain for a transistor.

6. A semiconductor device of claim 5 wherein said at least one source and at least one drain are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

7. A semiconductor device of claim 5 wherein said at least one source and at least one drain are laid out in a substantially checkerboard pattern.

8. A semiconductor device comprising:

a. semiconductor substrate;

b. at least one first doped region in said semiconductor substrate forming at least one source;

c. at least one second doped region in said semiconductor substrate forming at least one drain;

d. a first connectivity layer operatively connected to said at least one first doped region;

e. a second connectivity layer operatively connected to said first connectively layer and operatively connected to said at least one second doped region.

9. A semiconductor device of claim 8 wherein said second conductivity layer is operatively connected to said at least one second doped region through said first conductivity layer.

10. A semiconductor device of claim 9 wherein said second conductivity layer is operatively connected to said at least one second doped region through said first conductivity layer and using a portion of said first conductivity layer for such connection.

11. A semiconductor device of claim 8 having a third conductivity layer with at least one first pad and at least one second pad of such layer wherein said at least one first pad is operatively connected to said first connectivity layer and said at least one second pad is operatively connected to said second connectivity layer.

12. A semiconductor device of claim 11 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

13. A semiconductor device of claim 12 wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

14. A semiconductor device of claim 12 wherein said at least one first pad is interleaved with said at least one second pad.

15. A semiconductor device of claim 8 wherein said at least one source and at least one drain are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

16. A semiconductor device of claim 8 wherein said at least one source and at least one drain are laid out in a substantially checkerboard pattern.

17. A semiconductor device comprising:

a. semiconductor substrate;

b. at least one first doped region in said semiconductor substrate forming at least one source;

c. at least one second doped region in said semiconductor substrate forming at least one drain;

d. a first connectivity layer having at least one first runner operatively connected to said at least one first doped region and at least one second runner operatively connected to said at least one second doped region;

e. a second connectively layer having at least one first pad operatively connected to said at least one first runner and at least one second pad operatively connected to said at least one second runner.

18. A semiconductor device of claim 17 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

19. A semiconductor device of claim 18 wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

20. A semiconductor device of claim 18 wherein said at least one first pad is interleaved with said at least one second pad.

21. A semiconductor device of claim 17 wherein said at least one source and at least one drain are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

22. A semiconductor device of claim 17 wherein said at least one source and at least one drain are laid out in a substantially checkerboard pattern.